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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Applicant: Flynn	Art Unit: 2651
Serial No.: 10/706,254	Examiner: Tzeng
Filed: November 12, 2003	**HSJ920030243US1**
For: **SYSTEM AND METHOD FOR WRITING SERVO TRACK IN SEALED HDD**	December 26, 2005 750 B STREET, Suite 3120 San Diego, CA 92101

APPEAL BRIEF

Commissioner of Patents and Trademarks

Dear Sir:

This brief is submitted under 35 U.S.C. §134 and is in accordance with 37 C.F.R. Parts 1, 5, 10, 11, and 41, effective September 13, 2004 and published at 69 Fed. Reg. 155 (August 2004). This brief is further to Appellant's Notice of Appeal filed herewith.

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(1) Real Party in Interest

The real party in interest is Hitachi Global Storage Technologies, Netherlands, B.V.

(2) Related Appeals/Interferences

No other appeals or interferences exist which relate to the present application or appeal.

(3) Status of Claims

Claims 1-17 are pending, claims 3 and 4 have been indicated as being allowable, and Claims 1, 2, and 5-17 have been finally rejected, which rejections are hereby appealed. Claim 18 is canceled.

(4) Status of Amendments

No amendments are outstanding.

(5) Concise Explanation of Subject Matter in Each Independent Claim, with Page and Figure Nos.

As an initial matter, it is noted that according to the Patent Office, the concise explanations under this section are for Board convenience, and do not supersede what the claims actually state, 69 Fed. Reg. 155 (August 2004), see page 49976. Accordingly, nothing in this Section should be construed as an estoppel that limits the actual claim language.

Claim 1 recites a HDD that includes a write channel 46 having a write gate 44, figure 4, page 9, last three lines. Control circuitry that can be implemented in, e.g., actuator electronics 18 and/or a controller 20, figure 1, page 6, first two paragraphs encodes write control bits for controlling the write gate to selectively enable writing data bits associated with a servo pattern onto a disk 14, figure 1, page 6.

Claim 6 recites a method for self-writing a servo pattern to a disk 14, supra using a write channel 46, supra that is intended for subsequently writing user data. The method includes receiving a servo pattern defined by a stream of data bits, and associating write control bits with the servo pattern, with values of the write control bits indicating whether a write gate associated with the write channel is enabled or disabled, figure 3 and pages 7-9.

Claim 12 sets forth a system including a hard disk drive controller 20, supra, a disk 14, supra onto which the controller writes user data using a write channel 46 including a write gate 44, supra, and means (logic executed by 18 and/or 20, supra) for, at least prior to providing the system to the user, generating gate control means (e.g., write bits, supra) for selectively enabling and disabling the write gate while the write channel remains energized to write a servo pattern on the disk.

Claim 17 in contrast now recites a HDD that has a write channel 46, supra configured for writing user data to a disk and control circuitry (within the controller 20 and/or actuator 18, supra) determining a single write delay from a prior timing mark to indicate writing of a subsequent timing mark and a portion of a servo pattern, supra. A write gate 44 is in the write channel 46, and the write gate is controllable using write control bits generated by the control circuitry to selectively enable writing data bits associated with a servo pattern onto at least one disk, supra.

(6) Grounds of Rejection to be Reviewed on Appeal

(a) Claims 1 and 2 have been rejected under 35 U.S.C. §102 as being anticipated by Hussein, USPN 6,285,521.

(b) Claims 5 and 12-16 have been rejected under 35 U.S.C. §103 as being unpatentable over Hussein in view of Bryant et al., USPN 6,785,075 with "official notice" being resorted in the case of some of the claims under this section.

(c) Claims 6-11 and 17 have been rejected under 35 U.S.C. §103 as being unpatentable over Bryant et al. in view of Hussein with reliance on In re Rose being relied on for some of the claims in this section.

(7) Argument

As an initial matter, it is noted that according to the Patent Office, a new ground of rejection in an examiner's answer should be "rare", and should be levied only in response to such things as newly presented arguments by Applicant or to address a claim that the examiner previously failed to address, 69 Fed. Reg. 155 (August 2004), see, e.g., pages 49963 and 49980. Furthermore, a new ground of rejection must be approved by the Technology Center Director or designee and in any case must come accompanied with the initials of the conferees of the appeal conference, id., page 49979.

Additionally, Appellant notes for the record that the SPE initialed the last Office Action, indicating his concurrence. Accordingly, reopening prosecution now when all Appellant desires is Board review of the SPE-approved rejections would be egregious. Given that the SPE has gone on record as approving the present rejections being appealed, either allowance or an Examiner's Answer would appear to be the only two appropriate responses to this Appeal Brief.

(a) Hussein, figure 1 and col. 4, lines 34 and 35 and col. 5, lines 42-60 have been relied on as a teaching of controlling a write gate to selectively enable writing data bits associated with a servo pattern. This allegation is as pure a factual mistake as can be made. Nowhere does Hussein mention writing a servo pattern, something that ordinarily is done prior to vending the HDD. Indeed, Hussein appears to be directed to conventional disk operation. Thus, the disablement of the write gate by the servo controller discussed in col. 5 has nothing to do with writing data bits associated with a servo pattern as recited in Claim 1. The data written by Hussein is conventional client data, and the servo controller evidently is a conventional servo controller that coordinates slider positioning with data reading and writing, without having anything to do with writing a servo pattern.

Applicant notes that claims must be interpreted as one skilled in the art would interpret them, in light of the specification, MPEP §2111.01. As the Board is aware, the term "servo pattern" has a well-understood meaning in the art, and is something separate and distinct from the data that a client writes to a HDD. Nothing in the present specification leads away from this well-understood meaning. Accordingly, rejections based on allegations that Hussein has anything to do with writing servo patterns, much less by selectively enabling and disabling the write gate of the write channel of a HDD, much less still executing the selective enablement of the write gate responsive to write control bits in the servo pattern data being written, are overcome.

The examiner, bolstered by SPE support, has responded to the above accurate summary of the technology and the law by a flat-out misrepresentation, poorly worded. Specifically, the examiner has alleged that "claim is claiming conventional client data associated with a servo pattern. In other words, writing client data guided by servo directions provided from a servo pattern."

"The name of the game is the claim" - as actually written, not as incorrectly paraphrased by an examiner. Nowhere does Claim 1 recite "conventional" or "client data", much less "conventional client data". Nowhere does Claim 1 recite "writing client data". Nowhere does Claim 1 or the specification support the examiner's equating "writing client data guided by servo directions provided from a servo pattern" with "data bits ***that are associated with***" the servo pattern as claimed. All of these allegations are pure fabrications that deliberately ignore what the claim really says in a haphazard rush to rejection.

(b) The rejection of independent Claim 12 is interesting because of its internal inconsistency with the rejection of Claim 1 discussed above, because *apropos* Claim 12 the examiner now readily admits that Hussein fails to teach writing a servo pattern to disk prior to providing the disk to a user, resorting to Bryant et al., col. 1, lines 14-18 to supply the shortfall and alleging that this part of Bryant et al. "writes clock fields aligned in time and coherent in phase and frequency to servo pattern and clock fields previously written". Regardless of when the servo pattern is written in Bryant et al., it is not evidently done by selectively enabling and disabling the write gate while the write channel remains energized to write a servo pattern on the disk, as required by Claim 12. Since nothing in Hussein teaches doing anything at all related to servo writing, and since Bryant et al. does not appear to servo write as done in Claim 12, combining the references as proposed would result only in Bryant et al.'s conventional servo writing in combination with Hussein's subsequent non-servo writing - but not in Claim 12. For this reason, the rejections merit reversal.

Appellant further notes that in seeking to combine references, the name of the game is not the claim, but rather the requisite prior art suggestion to combine, MPEP §2143. The only rationale given for combining Hussein and Bryant et al. is because "they are from the same field of endeavor". Merely being

from the same field does not rise to the requisite prior art suggestion to combine, of course. Otherwise, the entire obviousness inquiry would reduce to a mere showing of analogousness under MPEP §2136, when in fact analogousness is nothing more than a threshold starting point for determining whether the subsequent analysis required under MPEP §2143 properly may be undertaken. The ensuing recognition by the examiner of why it would be useful to control the write gate using write control bits comes not from the relied-upon references, which nowhere consider it, but from a reading of the present specification. Since the present specification does not form part of the prior art, the references have been improperly combined.

This has been responded to by pretending that the Office Action does not in fact state that the references "are combinable because they are from the same field of endeavor" when in fact the rejections state just that several times. The examiner's response further points to col. 2, lines 30-32 of Hussein for the requisite motivation to combine. For the Board's convenience, here is the sum total of the "prior art evidence to combine" proferred by the examiner and SPE:

> "In addition, there is a need to reduce the power consumption in the spindle motor and its power MOSFETs without significantly increasing the recovery time to resume read and write operations after an idle period."

In other words, the relied-upon suggestion to combine appears to be beyond irrelevant to servo writing at all, and in fact approaches proving Appellant's point. As the section identified by the Examiner proves, Hussein is consumed with actual client data reads and writes. It is not at all related to writing servo patterns.

Elsewhere in the Office Action, Bryant et al., col. 2, lines 47-54 is relied on as the suggestion to combine. This section, however, merely discusses servo writing principles, which as stated above is inapposite to Hussein. In any case, in light of the absence of a legitimate prior art reason to combine the references, the rejections merit reversal.

Claims 14 and 15 have been rejected based on the two references discussed above in combination with "official notice". Appellant hereby incorporates by reference into this brief its previous discussion of MPEP §2144.03. Suffice it to say that the discussion has been ignored, along with Appellant's prior seasonable request under MPEP §2144.03 for a prior art showing of the allegedly well-known fact. For this reason, the rejections of these claims further merit reversal.

(c) Claim 6 recites self-writing a servo pattern to a disk using a write channel intended for subsequently writing user data, and goes on to specify that values of write control bits indicate whether a write gate associated with the write channel is enabled or disabled. Accordingly, Claim 6 requires using the write channel and write gate for servo self-writing that subsequently are used to write user data.

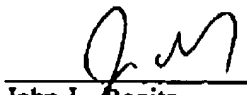
That is not, however, how Bryant et al. works. Instead, when servo self-writing, Bryant et al. uses a channel and presumably a gate that are different from the ones used for writing user data, col. 8, lines 10-18 (the mux 178 switches off the data write circuit portion 186 in favor of the pattern generator circuit 176, while using the data read portion). In fact, the rejection admits as much, resorting to the above-discussed portions of Hussein to remedy the shortfall. But as discussed above, Hussein is not directed to servo pattern writing at all, so the allegation that it controls a write gate to write a servo pattern is incorrect. In other words, combining the references as proposed would not arrive at Claim 6.

The rejection of Claim 7 (reciting that a write control bit is associated with at least one data bit) as well as Claims 8 and 9 is likewise legally deficient, being based on an admission that while the relied-upon references fail to teach it, it nonetheless would have been obvious based on a "change of size" theory. The reliance on Rose is inapposite. Applicant is not claiming a differently-sized element that is otherwise shown in the prior art. Applicant is claiming a specific relationship between a write control bit and a data bit. Relationships between data elements are not sizes. For the same reason, the rejections of Claims 8 and 9 on the same basis are overcome.

In the most recent Office Action, the SPE and examiner have not seen fit to respond to this argument or to explain why Appellant is wrong, probably because Appellant is right. The rejections merit reversal.

Next considering Claim 17, for reasons advanced above amended Claim 17 is patentable.

Respectfully submitted,



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APPENDIX A - APPEALED CLAIMS

1. A HDD, comprising:

at least one write channel including at least one write gate; and

control circuitry encoding write control bits for controlling the write gate to selectively enable writing data bits associated with a servo pattern onto at least one disk.

2. The HDD of Claim 1, wherein the write channel is used during operation to write user data to the disk.

3. The HDD of Claim 1, wherein the control circuitry encodes two bits of a ten bit parallel bus to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

4. The HDD of Claim 1, wherein the control circuitry encodes four bits of an eight bit parallel bus to indicate whether the write gate should enable writing one or more of the remaining four bits of the bus to disk.

5. The HDD of Claim 2, wherein the control circuitry determines a write delay to a next timing mark based on a current timing mark, the time delay including a clock cycle component and a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

6. A method for self-writing a servo pattern to a disk using a write channel intended for subsequently writing user data, comprising:

receiving a servo pattern defined by a stream of data bits; and

associating write control bits with the servo pattern, values of the write control bits indicating whether a write gate associated with the write channel is enabled or disabled.

7. The method of Claim 6, wherein a write control bit is associated with at least one data bit.

8. The method of Claim 7, wherein a write control bit is associated with one and only one data bit.

9. The method of Claim 7, wherein a write control bit is associated with at least two data bits.

10. The method of Claim 6, comprising writing the servo pattern on the disk after the disk has been sealed in a housing.

11. The method of Claim 6, further comprising:

determining a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component; and

using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

12. A system, comprising:

a hard disk drive controller;

at least one disk onto which the controller writes user data using at least one write channel, the write channel including a write gate; and

means for, at least prior to providing the system to the user, generating gate control means for selectively enabling and disabling the write gate while the write channel remains energized to write a servo pattern on the disk.

13. The system of Claim 12, wherein the gate control means include write control bits.

14. The system of Claim 13, wherein two write control bits of a ten bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

15. The system of Claim 13, wherein four bits of an eight bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining four bits of the bus to disk.

16. The system of Claim 12, comprising control circuitry determining a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and

a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

17. A HDD, comprising:

at least one write channel configured for writing user data to a disk;

control circuitry determining a single write delay from a prior timing mark to indicate writing of a subsequent timing mark and at least a portion of a servo pattern; and

at least one write gate in the write channel, the write gate being controllable using write control bits generated by the control circuitry to selectively enable writing data bits associated with a servo pattern onto at least one disk.

APPENDIX B - EVIDENCE

None (this sheet made necessary by 69 Fed. Reg. 155 (August 2004), page 49978.)

APPENDIX C - RELATED PROCEEDINGS

None (this sheet made necessary by 69 Fed. Reg. 155 (August 2004), page 49978.)